SIGE BICMOS CIRCUIT AND SYSTEM DESIGN AND CHARACTERIZATION FOR EXTREME ENVIRONMENT APPLICATIONS

A Thesis
Presented to
The Academic Faculty

by

Troy England

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2011

SIGE BICMOS CIRCUIT AND SYSTEM DESIGN AND CHARACTERIZATION FOR EXTREME ENVIRONMENT APPLICATIONS

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To my Lord and Savior, Jesus Christ.

May everything I do be worship unto You.

ACKNOWLEDGEMENTS

I wish to thank my incredible better half, Ashley Cobb. Her patience and love has kept me sane during the most trying times of this work. I wish to thank my family for their constant support and encouragement. I want to thank my advisor, Dr. John Cressler, for his guidance and faith in me. I also wish to thank the rest of the SiGe Device and Circuit research team for the ever-enlightening discussions, Christina Bourgeois and Michael Laughter for making a Writing TA out of me, the other NASA ETDP team members for their support, and Dr. Gregory Durgin and Dr. John Papapolymerou for being on my thesis reading committee.

This work was supported by NASA ETDP under contract NNL06AA29C.

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SUMMARY

This thesis describes the architecture, verification, qualification, and packaging of a 16-channel silicon-germanium (SiGe) Remote Electronics Unit (REU) designed for use in extreme environment applications encountered on NASA's exploration roadmap. The SiGe REU was targeted for operation outside the protective electronic "vaults" in a lunar environment that exhibits cyclic temperature swings from –180ºC to 120ºC, a total ionizing dose (TID) radiation level of 100 krad, and heavy ion exposure (single event effects) over the mission lifetime. The REU leverages SiGe BiCMOS technological advantages and design methodologies, enabling exceptional extreme environment robustness. It utilizes a mixed-signal Remote Sensor Interface (RSI) ASIC and an HDL-based Remote Digital Control (RDC) architecture to read data from up to 16 sensors using three different analog channel types with customizable gain, current stimulus, calibration, and sample rate with 12-bit analog-to-digital conversion. The SiGe REU exhibits excellent channel sensitivity throughout the temperature range, hardness to at least 100 krad TID exposure, and single event latchup immunity, representing the cutting edge in cold-capable electronic systems. The SiGe REU is the first example within a potential paradigm shift in space-based electronics.

The novelty of this work is the comprehensive, ground-up generation of new extreme environment design methodologies, culminating in the creation of a new state-of-the-art system-in-package that, for the first time, enables decentralized electronics throughout space-based vehicles without temperature control or shielding. The implication is that the elimination of restrictive, wasteful wiring and protection schemes will enable lighter and more capable space-based systems. This author is also a co-author and primary author, respectively, of two of the largest publications to come about from this effort:

R. M. Diestelhorst, et al., "A New Approach to Designing Electronic Systems for Operation in Extreme Environments: Part I - The SiGe Remote Sensor Interface," *IEEE Aerospace and Electronic Systems Magazine*, in press

T. D. England, et al., "A New Approach to Designing Electronic Systems for Operation in Extreme Environments: Part II - The SiGe Remote Electronics Unit," *IEEE Aerospace and Electronic Systems Magazine*, in press

CHAPTER 1

INTRODUCTION

Electronics in space vehicles face a host of challenges from their harsh operating environment. Extremely wide temperature ranges and dangerous levels of cosmic and trapped radiation can cause catastrophic damage to unprotected circuitry. Traditionally, “warm-boxes” or “electronics vaults” have provided the shielding and heating necessary to protect crucial components. Unfortunately, these solutions come with a high cost in weight, volume, power, and complexity as shown in Figure 1 [1].

Figure 1. The radiation vault for NASA’s Juno spacecraft weighed 500 pounds

Recently, there has been a paradigm shift that advocates moving away from centralized “warm-boxes” and towards de-centralized system-on-a-chip and system-in-a-package solutions that do not require environmental control. SiGe BiCMOS technology is one of the factors driving this shift because it provides excellent over-temperature

performance, built-in total ionizing dose (TID) and displacement damage (DD) radiation tolerance, and 100% compliance with standard Si manufacturing processes. Consequently, in 2005, NASA began the "SiGe Integrated Electronics for Extreme Environments" project. They brought together six universities, four companies, and one government laboratory to develop an infrastructure to demonstrate that SiGe BiCMOS (SiGe HBT + CMOS) technology was a viable candidate for implementing extreme environment electronics, particularly targeting future missions to the Moon and Mars [2]. This team used IBM's SiGe 5AM process to create a library of circuit blocks of all types (analog, digital, RF, and mixed-signal) and validated them over temperature (–180 to +120°C) and against both TID and Single Event Latchup (SEL) radiation damage [3, 4].

As a final proof-of-concept, the team designed and fabricated the SiGe Remote Electronics Unit (REU), which is made up of two ASICs, the Remote Sensor Interface (RSI) and Remote Digital Control (RDC). Contained within the RSI ASIC were a total of 16 instrumentation channels of three different types, universal, high-speed, and charge, and a 16 channel, multiplexing, Wilkinson ADC.

This thesis presents a full view of the SiGe Remote Electronics Unit (REU) and over-temperature and radiation testing results of the RSI ASIC with an FPGA-based implementation of the RDC functionality. Specifically, it presents chapters on SiGe technology in extreme environments, the REU legacy architecture, the RDC functionality, REU system validation methods, the over-temperature experimental qualification of the RSI ASIC with RDC-based FPGA, the radiation qualification of the same, the packaging of the dual-ASIC, multi-chip module (MCM) REU, mission insertion opportunities for the SiGe REU, and finally, some concluding remarks.

CHAPTER 2

SIGE TECHNOLOGY FOR EXTREME ENVIRONMENTS

An enabling force behind the shift to localized, minimally shielded electronics in space-based systems is the flexibility of SiGe BiCMOS technology, specifically the SiGe HBT, to tolerate the extreme conditions presented by extra-terrestrial environments. As the SiGe HBT approaches cryogenic temperatures, the most important device metrics for circuit design improve: current gain, transconductance, f_T, f_{MAX}, and broadband noise [5]. Instead of spending size, weight, and power to keep electronic systems heated, designers can leverage the cold-capability of the SiGe HBT to improve system metrics and operate robustly at cryogenic temperatures. SiGe HBTs have been shown to be robust not only at 77 K but down to 300 mK [6-9]. Because the SiGe HBT is so well-suited for the low temperature regime it is easy to falsely assume it cannot be utilized at high temperatures; however, high temperature SiGe electronics are presently under development. For instance, a SiGe HBT-based voltage reference in [10] has been demonstrated for operation up to 300°C. Thus, the SiGe HBT has emerged as a viable contender for ultrawide-temperature applications.

Additionally, the SiGe HBT has a natural, built-in resistance to TID and DD radiation effects that can be explained by aspects of the device structure. First, against TID, the extrinsic base of the transistor is very heavily doped. Second, the extrinsic base is located underneath an oxide/nitride composite, which is known to exhibit increased radiation immunity. In addition, the volume of the SiGe HBT is extremely small and highly doped, making it less susceptible to DD [11]. Previous data has shown that newer generation SiGe HBT devices are hardened against major degradations in current gain in mid- and high-injection to multiple Mrad and have even higher TID tolerance at cryogenic temperatures [12]. The SiGe HBT thus shows great promise in being the

cornerstone of space electronics due to its robustness against temperature variation and tolerance to radiation exposure.

CHAPTER 3

REMOTE ELECTRONICS UNIT

BAE Remote Health Node

The SiGe Remote Electronics Unit (REU) is a miniaturized version of the key functionality of the Remote Health Node (RHN) originally developed in the 1990s for the NASA X-33 space plane. The X-33 program was an experimental spacecraft for the reusable launch vehicle program. The RHN was a key component of the integrated vehicle health management (IVHM) system [13]. In the X-33 platform, the IVHM system consisted of a pair of central vehicle management computers and fifty of the RHN units distributed around the periphery of the X-33 to gather telemetry from a wide variety of sensors, as shown in Figure 2.

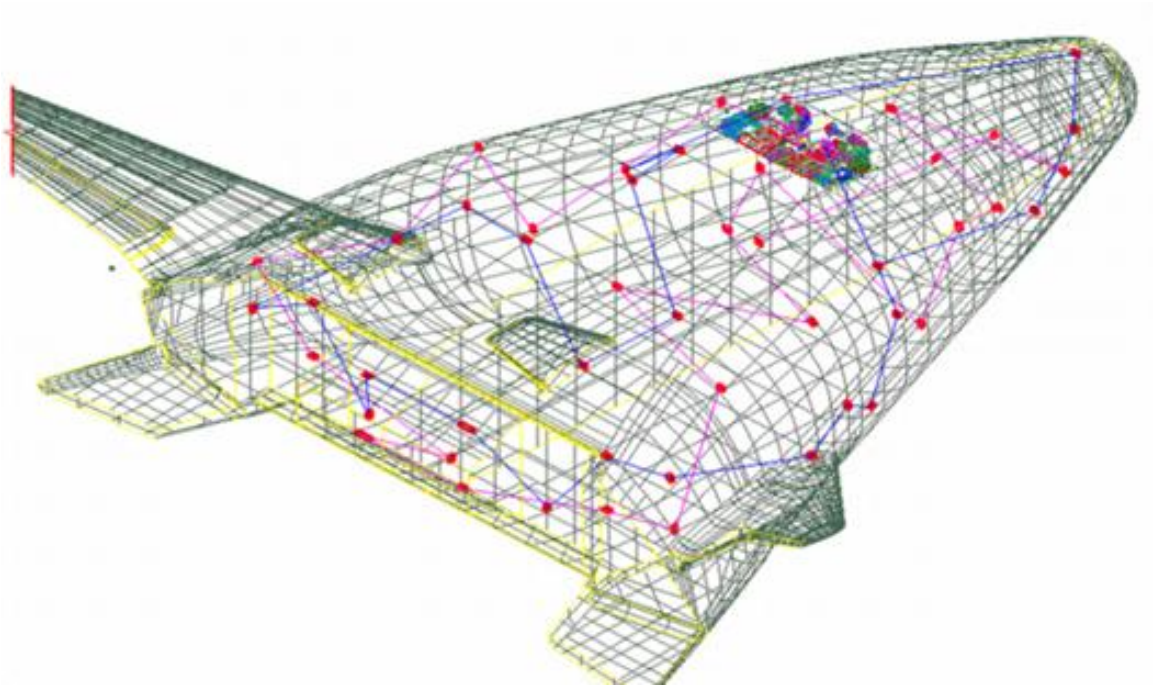

Figure 2. X-33 space plane showing distributed RHN locations

The RHN unit, shown in Figure 3, weighed 5 pounds, with a volume of just over 101 cubic inches, and dissipated 17 W of power.

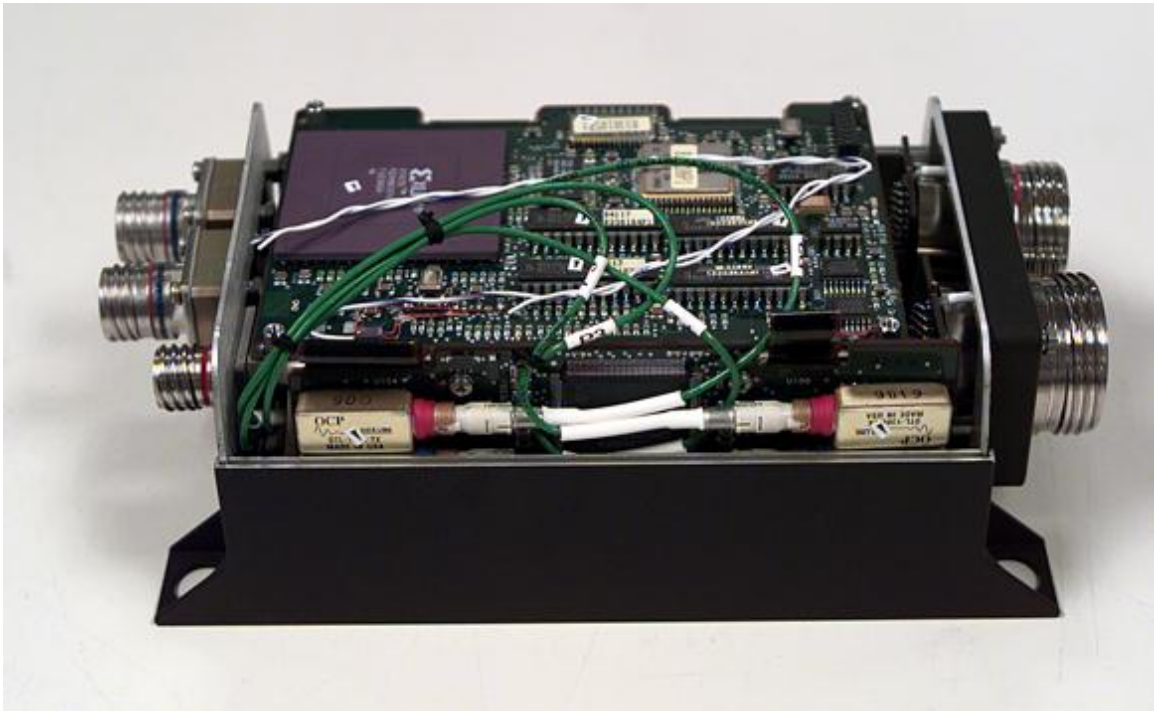

Figure 3. The original BAE Remote Health Node

It accepted inputs from as many as 40 sensors through several different types of processing channels via a pair of large multi-pin connectors located on one end of the box. The front-end channels were comprised of discrete analog circuits assembled into hybrid modules. Following digitization, the collected information was transmitted to the central computers via a pair of Health Optical Buses (HOB) employing the Fiber Distributed Data Interface (FDDI) protocol. Each computer supported 25 of the RHN boxes [14].

RSI-with-FPGA Remote Electronics Unit

The Remote Sensor Interface (RSI) ASIC is a consolidation of the three primary channel types from the RHN box along with analog-to-digital conversion [15]. There are a total of 16 channels, organized as twelve universal channels with selectable Wheatstone

bridge configuration inputs supporting sensors with a data rate up to approximately 200 Hz, two higher data rate (up to 5 kHz) channels with an asymmetric bridge configuration, and two channels that accept piezoelectric transducer inputs. Some of the channels incorporate special circuitry based on high voltage transistors on the input stages to accommodate high voltage (up to 12 V) sensors. A block diagram of the RSI is shown in Figure 4.

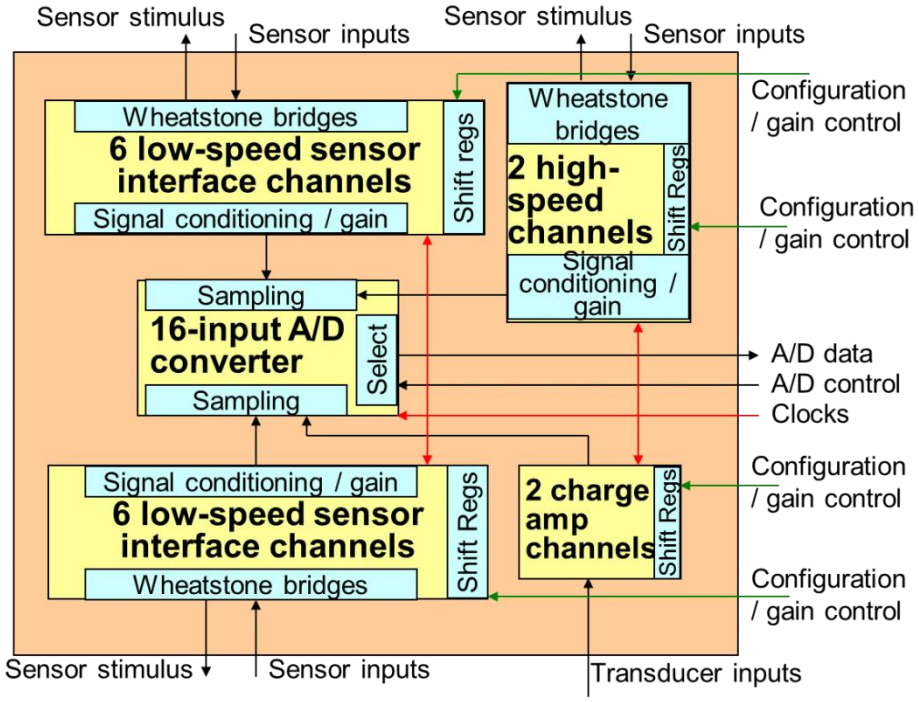

Figure 4. Simplified block diagram of the Remote Sensor Interface ASIC

Each of the channels is configured from the digital control section of the REU. Each channel type includes a set of serially loaded shift registers that are loaded with configuration settings during the initialization process and then remain static during REU operation. An additional set of shift registers feeds data into the digital-to-analog converters that are then used to calibrate the analog channels. The configuration registers employ Radiation Hardening by Design (RHBD) techniques to minimize the possibility of particle-induced data corruption. Following signal conditioning in the form of bridge

configuration and gain control, the analog signals are digitized in parallel using a 12-bit, Wilkinson architecture, analog-to-digital converter (ADC) and then are multiplexed in the Remote Digital Control (RDC) for sample averaging. A block diagram of the RDC is shown in Figure 5.

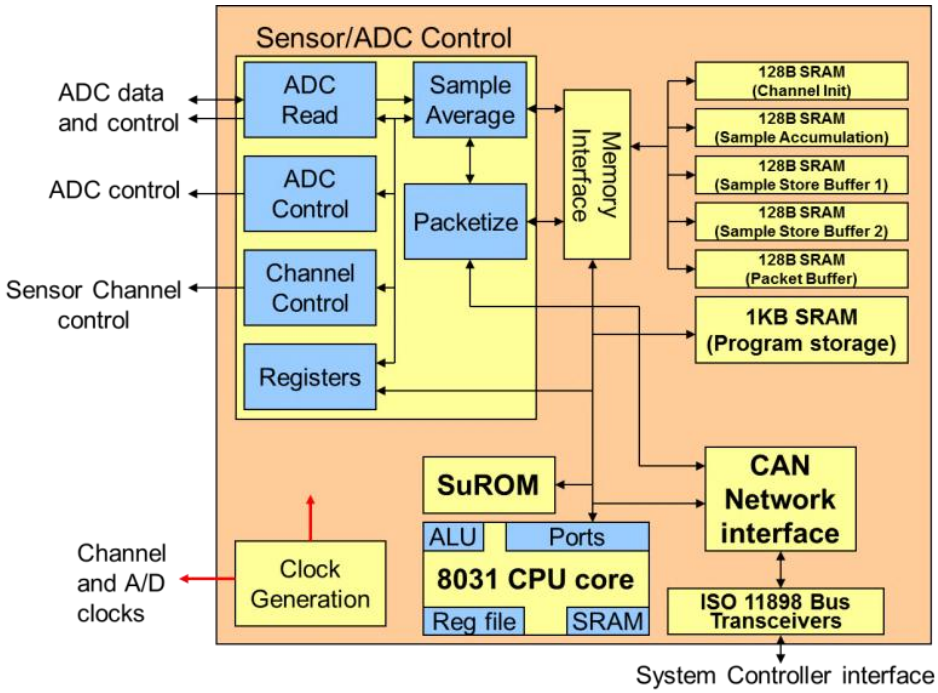

Figure 5. Simplified block diagram of the Remote Digital Control ASIC

The averaged data samples undergo packetization into Controller-area Network (CAN) bus packets [16] for transmission to the central computer, a process which includes appending a time stamp. The CAN-bus replaces the FDDI optical data bus employed on the original RHN unit. Note that the ISO 11898 transceivers are external to the FPGA version of the RDC because they are unique circuits, but they are embedded into the ASIC implementation.

CHAPTER 4

REMOTE DIGITAL CONTROL

Architecture

The RDC is an HDL-based, CPU and finite-state machine (FSM) driven system that reads, processes, and sends the samples from the RSI chip to a central system via the CAN-bus over an ISO 11898 physical layer. Figure 5 includes an overview of the RDC's architecture. In addition to the CPU and CAN related circuits, the RDC contains register configurable FSMs for CAN-packet building and RSI sample processing and storage elements for CPU instructions, processed samples, and configuration data for all 16 RSI channels.

The CPU design is based on the 8031 microcontroller architecture but is implemented using NULL Convention Logic (NCL) [17]. Asynchronous logic of this type has the advantage of being functional across many variation types: process, voltage rail, temperature, etc. This particular module has been shown previously to function down to a voltage rail of 0.36 V or temperatures down to 4 K [18], making it ideal for extreme environment applications.

Functionality

The RDC follows a certain sequence of operation, divided into the start-up and execution phases. After power-up and reset, it goes into start-up where it sets up the CAN-bus interface and broadcasts a message to all other CAN-bus devices, including the system controller, to indicate its presence on the bus. The system controller then sends commands over the CAN-bus, programming the 8031 for execution and selecting values for the RSI channel settings.

During execution, the RDC sends control signals to the RSI's channel and ADC interfaces and receives raw digital samples from each of the 16 channels through the ADC. FSMs then process the samples on a per-channel basis (Figure 6).

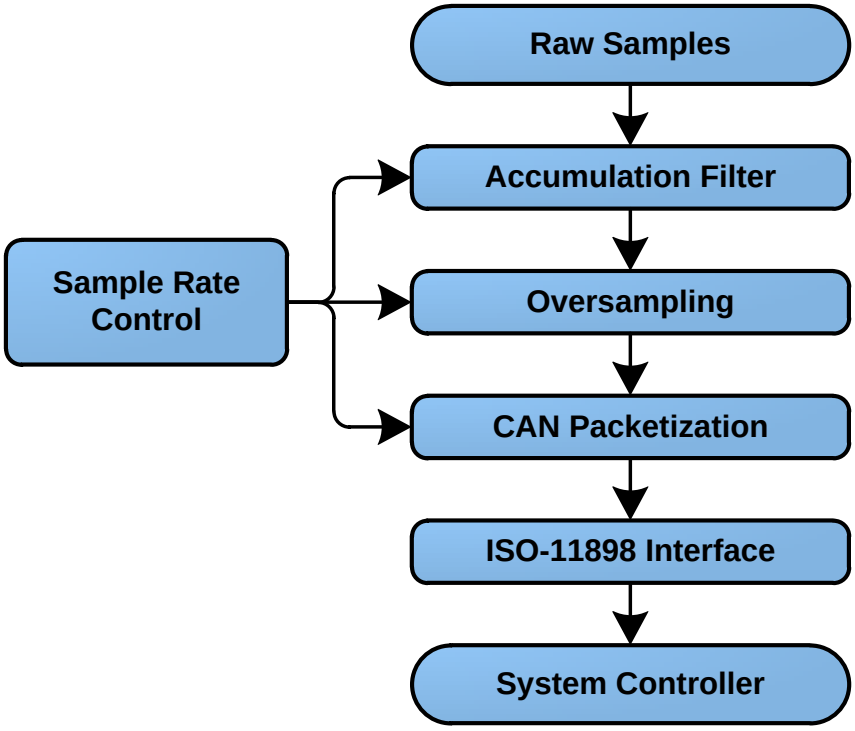

Figure 6. Flow diagram of the sampled data from the ADC to the system controller

An accumulation filter selects which samples to save based on the accumulation ratio defined by the programmed sample rate for that channel. For example, a 1:8 accumulation ratio means for every eight raw samples received from a channel, one will be kept and seven will be ignored. In this way, the CAN-bus is not over-crowded with unnecessary data.

The selected raw samples converge in oversampling, the next stage of the sample pipeline. Here, samples are averaged together based on a given over-sample ratio that is also defined by the sample rate of each channel. As a second example, a 32:1 over-sample ratio means 32 raw samples are used to produce an averaged sample. Next, an FSM builds the averaged samples into CAN data packets for eventual transmission to the

system controller. Once ready, those packets are transmitted over the CAN-bus to the system controller.

Remote Digital Control ASIC

A fully-functional RDC ASIC has been designed and is currently in fabrication. A screen capture of the ASIC layout can be seen in Figure 7. As a part of its development, a prototype was first programmed into a Xilinx® FPGA on a test board. It offered a hardware environment for verifying the feasibility and correctness of the overall RDC architecture. The FPGA itself was loaded with the RDC's HDL code; however, the FPGA did not include NCL logic, so it required a Boolean logic version of the 8031 CPU. This FPGA implementation was used alongside the RSI ASIC for the over-temperature and radiation testing presented here.

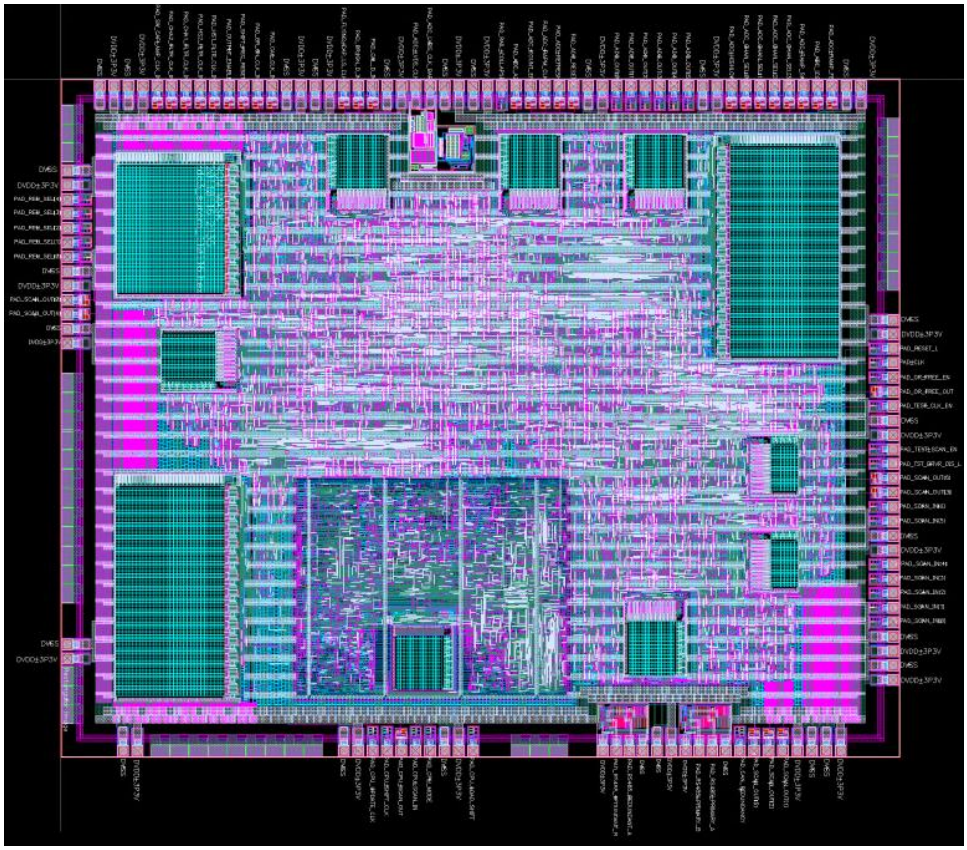

Figure 7. Cadence® screen capture of the latest version of the RDC ASIC

CHAPTER 5

VERIFICATION OF THE REMOTE ELECTRONICS UNIT

Verification of the two-ASIC (RSI + RDC) REU presented significant challenges. First, each chip was complex in its own right. The RSI contained nearly 300,000 analog/mixed-signal devices and over 167,000 nodes. Full chip analog simulation times were measured in days, not hours. Second, the REU constituted a true system-in-a-package (SiP), integrating the two large ASICs onto a uniquely designed substrate with numerous off-chip passive components. Next, each ASIC followed a very different design flow. The RSI, being heavily analog in circuit content, relied on schematic capture and Cadence® Spectre® simulations, while the RDC, being largely digital in content, was based on RTL code and Mentor Graphics® QuestaSim simulations. A creative means of implementing system level simulations accurately and efficiently was required.

The team used a technique called Event-Driven Mixed- Signal (EDMS) modeling [19]. The basic principle of this technique was to create analog models that could be consumed by digital simulators [20]. The team created the Event-Driven Mixed-Signal Design and Verification Studio, which contains libraries of EDMS effects to graphically assemble analog models that ran with high fidelity on a digital simulator. The impact of this technique on REU level verification was extraordinary, in that the simulation times were 100X-1,000X faster than transistor level simulations. Examples are shown in Table 1.

Table 1. Comparison of simulation times for selected RSI blocks

	Analog	*EDMS*	*Factor*
RC Filter	25.56 s	1.27 s	30x
6^{th} Order Butterworth Filter	31 min.	14 s	130x
Wilkinson ADC	8 hr.	33 s	870x

EDMS model fidelity was a key issue, as it intentionally abstracted RSI channel level behaviors from transistor-level detail. The team identified the major channel level behaviors required to support REU level functional verification:

- I/O and connectivity equivalence
- Supply domain sensitivity
- Polarity of all digital signals, control, gain, calibration
- Clocking behavior and clocking frequencies
- Bandwidth and delay related behaviors
- Dynamic threshold and dynamic range behaviors
- Voltage and current relationships for sensor bridges

The approach to validating the EDMS models was simple. Analog stimuli from the channel level test benches were “replayed” within the corresponding EDMS model test benches. Validation of each model was complete when the results matched. Any discrepancy between results was eliminated by modifying the behavior of the EDMS models, either by including addition effects or modifying effect parameters.

With EDMS replay effects, REU level results could be re-used as stimulus for the channel level verification simulations in Spectre, creating a new level of observation into RDC and RSI interactions for both the digital and analog design teams. The RDC RTL code and test bench were merged with the RSI EDMS models in an REU level test bench. This test bench included re-configurable sensor loads to rigorously exercise the REU chip-set (Figure 8).

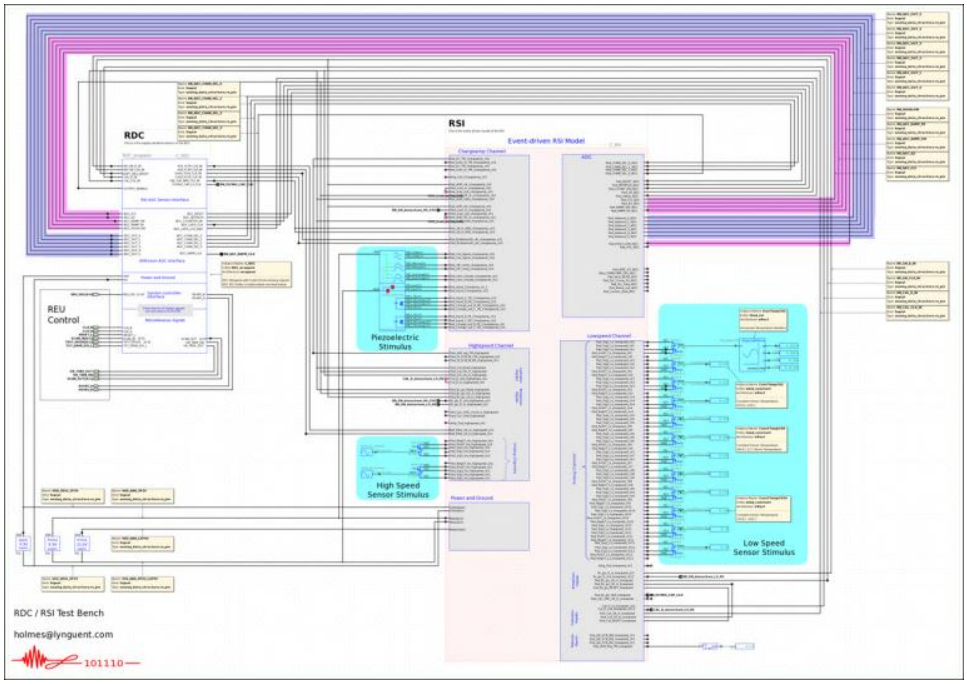

Figure 8. Combined RDC and RSI (REU Level) EDMS model test bench

The active sensor models provide the means for designers to evaluate the REU in a simulation of any conceivable mission profile. The final milestone of REU level verification was the successful demonstration of sensor waveforms appearing as CAN packets on the ISO 11898 interface seen in Figure 9.

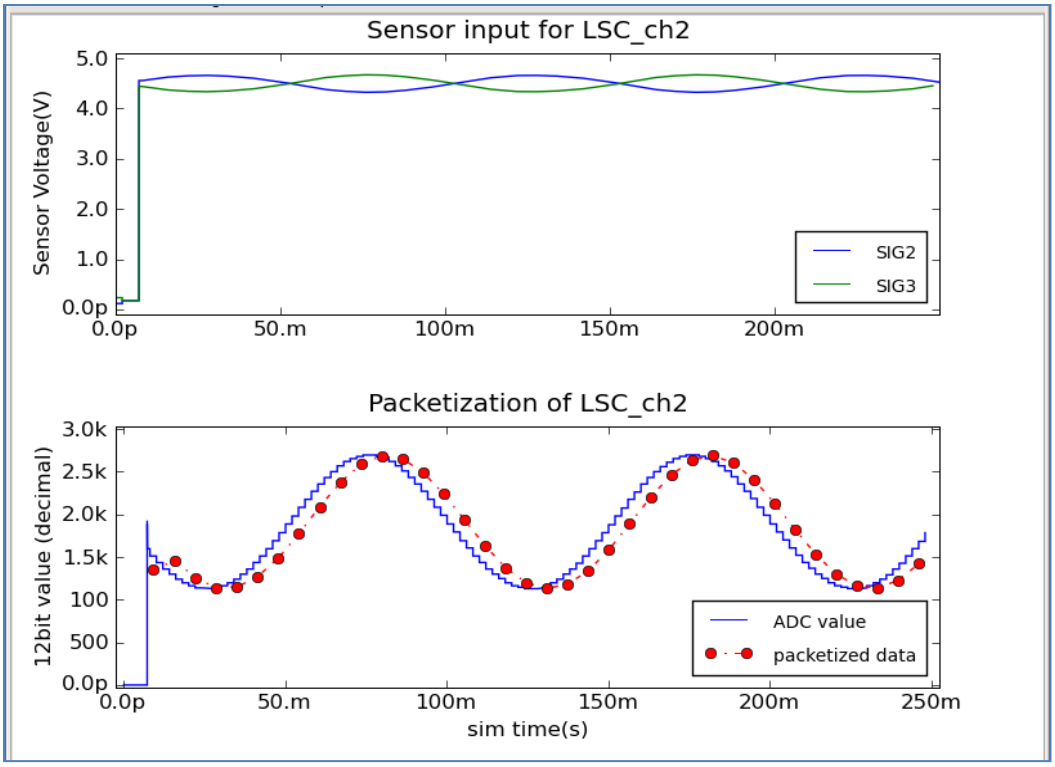

Figure 9. An EDMS model simulation of end to end data over the CAN-bus

CHAPTER 6

RSI-WITH-FPGA REMOTE ELECTRONICS UNIT WIDE TEMPERATURE TESTING

Over-temperature and Radiation Test Dewar

A cryogenic dewar customized for single-event testing [21] was used for carrying out the experiments reported in this paper; it appears in the center of Fig. 9.

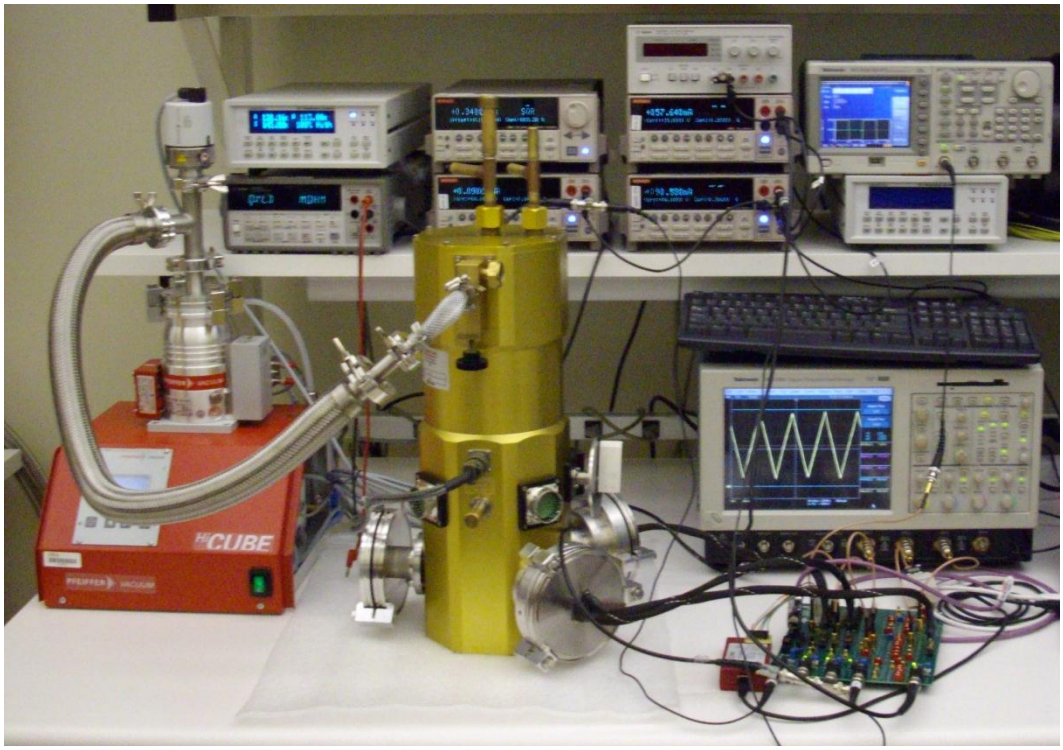

Figure 10. The over-temperature experimental set-up

The dewar can be used with LN2 (boiling point –196°C) or LHe (boiling point –269°C) as cryogens, depending upon the lowest temperature desired. Six hermetically sealed ports on the dewar provide ample choice for a variety of electrical connection configurations, such as hermetic 61-pin connectors for dc measurements or customized hermetic high speed feedthroughs for transient capture [21]. Two of these ports were

fitted with customized vacuum-sealed flanges, each mounted with multiple 25-pin electrical micro-D subminiature (MDM) feedthroughs. A mechanical heat switch enables control over the amount of heat transfer between the dewar/DUT and the external world.

The beam port of the dewar is flange adaptable to match that of the broad beam line at the test facility. At the Texas A&M University Cyclotron Institute, the dewar beam port was adapted with a hermetically sealed Aramica window flange similar to the one on the beamline. The RSI daughter card and the DUT mounted on it were designed such that the center of the DUT corresponded to the central axis of the beamline. All dewar measurements were carried out at a normal angle of incidence.

The DUT was cooled using a custom-designed copper cold finger that was in contact with both the DUT and the dewar cryogen vessel. Temperature sensors were placed on the cold finger and the dewar vessel to monitor the respective temperatures simultaneously through an external Lakeshore 331S temperature controller. The controller was used to regulate the heat applied to the system through a 50 W heater attached to the dewar vessel, and thus facilitate single-event testing over temperature.

Test Board Design

Test board design for the RSI was constrained primarily by the radiation test dewar. A two-board solution was chosen with the goal of keeping the maximum amount of the supporting commercial circuitry at room temperature. The in-dewar daughter card held the RSI and FPGA-based RDC. Outside the dewar, the motherboard contained all the power management and interface circuitry.

Daughter Card

The internal volume of the test dewar and availability of low thermally conductive, cryogenic ribbon cable drove the design process of the daughter card. Using nearly all the available space, the board was 4.25” x 4.00” and consisted of the RSI in a

256 pin grid array package, a Xilinx® Spartan® 3E 1200 FPGA, three MDM cable headers for the primary cabling, a 3 x 12 grid of pin headers for optional diagnostic signals, multiple sets of power rail decoupling capacitors, necessary off-chip passives for the charge channels and the ADC, and optional fixed resistors at the inputs of the high-speed and universal channels, as seen in Figure 11.

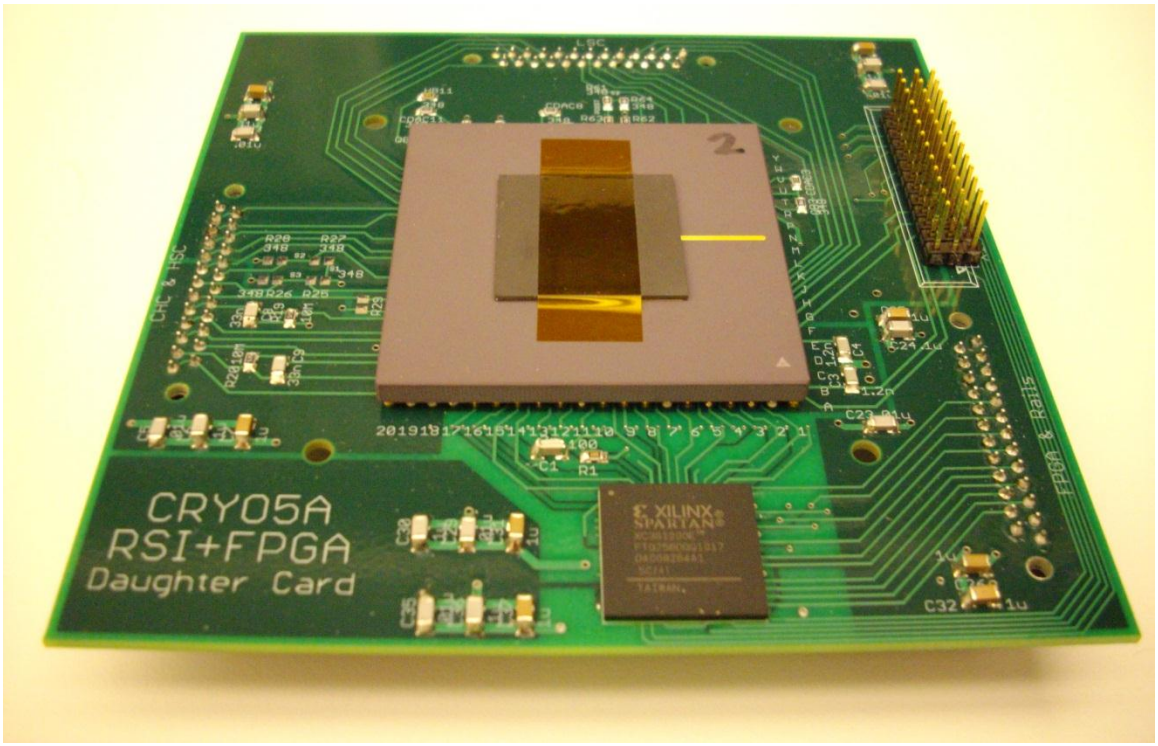

Figure 11. The RSI-with-FPGA REU in-dewar daughter card

While in the dewar, a limited number of conductors could be used between the daughter card and outside world because each one created a thermal shunt from the RSI, limiting the testing temperature range. Unfortunately, the thermally resistive cryogenic conductors also had a series electrical resistance of approximately 50 Ω, so one of the three cables had to be a thermally conductive copper cable for rail current handling. The low conductor count also meant that only half of the 16 channels were accessible for testing, but at least two of each type were represented.

During over-temperature measurements, the three internal MDM cables connected from the daughter card to dewar flanges and on the outside, another set of copper MDM cables connected to the motherboard. Shorting jumpers were used on the 100 mil daughter card headers to set the optional test signals to predefined DC values. When out of dewar, the three MDM cables connected directly to the motherboard, and a 26-pin ribbon cable made the diagnostic signals available for use on the motherboard.

Motherboard

The motherboard contained all of the power management and interface circuitry. Five different programmable voltage regulators, each with sets of decoupling capacitors, ensured a clean voltage supply to the daughter card. Commercial ISO 11898 transceivers were used for CAN-bus communication. Pin headers were used with a USB JTAG adapter to program the FPGA. DIP switch arrays made it possible to present various Wheatstone bridge configurations and load resistances to the universal and high-speed channels. A photograph of the motherboard is shown in Figure 12.

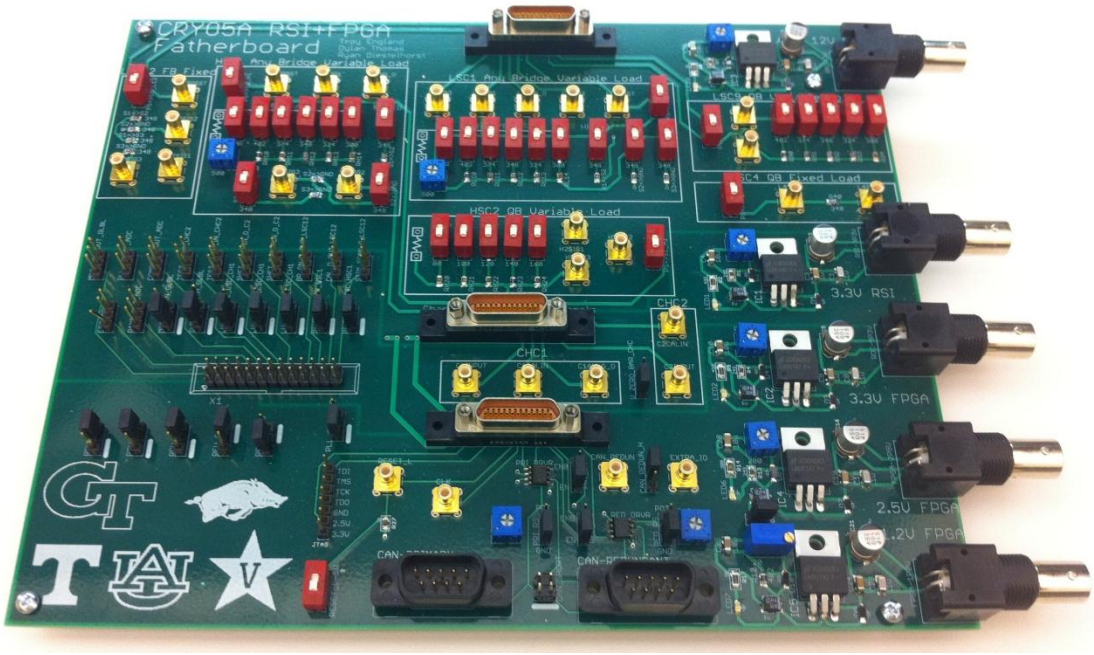

Figure 12. The RSI-with-FPGA Remote Electronics Unit motherboard

Measurement Methods

The main measurement objective was a quantification of resolution, noise level and system sensitivity over temperature. Resolution was defined as the amount of change of the measured element per least significant bit (LSB) of the ADC. In the case of the universal and high-speed channels the element was resistance, and thus the resolution can be expressed as in (1). The ADC output was saved versus five different values of the input resistor, and a linear regression fit was used to derive the resolution.

$$Resolution\left(\frac{\Omega}{LSB}\right) = \frac{\Delta R_L}{\Delta LSBs} \tag{1}$$

The charge channel required special consideration because precisely controlling the charge at the input node was very difficult. Instead, a sine current source was used at the input to precisely control the change in charge over time, ΔQ. Taking advantage of the integral relationship between current and charge in (2) and analyzing the ADC output made the calculation of (3) possible.

$$\Delta Q = \int_0^{\frac{1}{2f}} Acos(2\pi ft)dt = \frac{A}{\pi f} \tag{2}$$

$$Resolution\left(\frac{Q}{LSB}\right) = \frac{\Delta Q}{\Delta LSB} \tag{3}$$

Next, noise analysis information was needed. Grounding the inputs of each channel constituted an invalid state, so another approach was required. The best strategy was to create a standard DC output on each channel and take a transient measurement. For the universal and high-speed channels, a balanced 350 Ω Wheatstone bridge was connected to the input, ensuring the measured differential voltage was zero, and resulting in 600 mV at the output. For the charge channel a built-in ability to short internal

feedback was used to produce a DC voltage on the output. Approximately five seconds worth of ADC samples were saved per measurement in these states.

The standard deviation of the set of samples was taken as the AC-coupled measurement of RMS noise in units of LSBs because the standard deviation of a set of values is equivalent to the RMS about the mean of the set. Sensitivity was then defined as the input referred noise floor of each channel. By multiplying the values of resolution and noise, the equivalent output noise source can be referred back to the measured unit in RMS, as indicated in (4) and (5).

$$Sen.(\Omega) = Noise\ (LSBs) \times Res.\left(\frac{\Omega}{LSB}\right) \tag{4}$$

$$Sen.(Q) = Noise\ (LSBs) \times Res.\left(\frac{Q}{LSB}\right) \tag{5}$$

Resolution, Noise and Sensitivity Results

The methods discussed in the previous sub-section were performed for multiple gain states during over-temperature testing from 100 K to 343 K. The results of resolution measurements are shown in Figures 13–15.

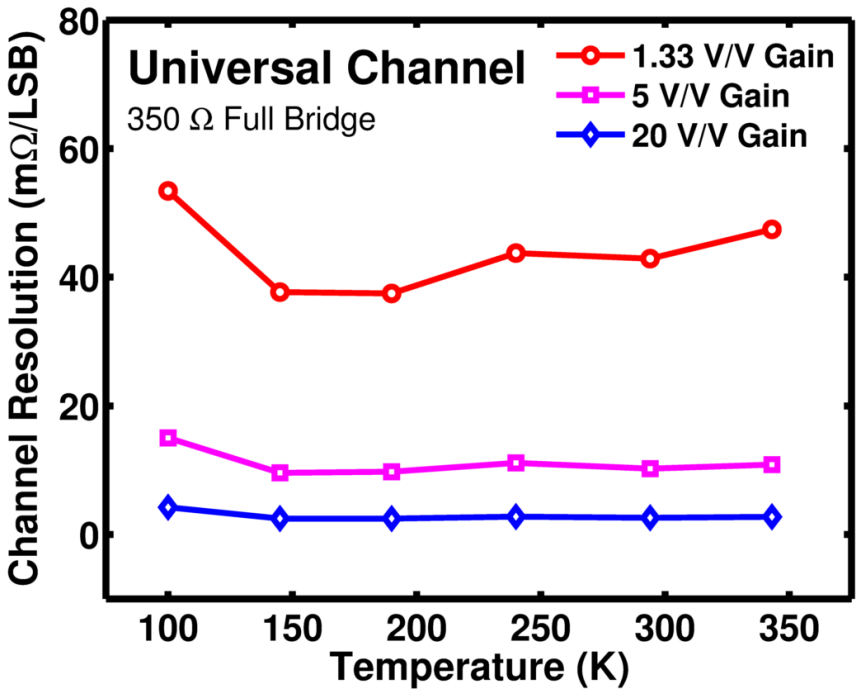

Figure 13. The universal channel resolution

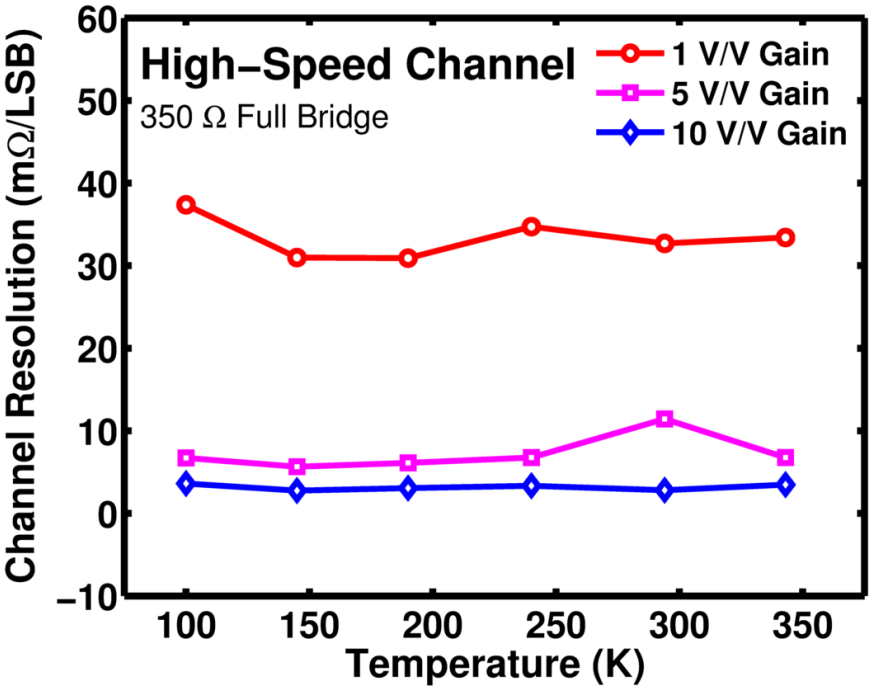

Figure 14. The high-speed channel resolution

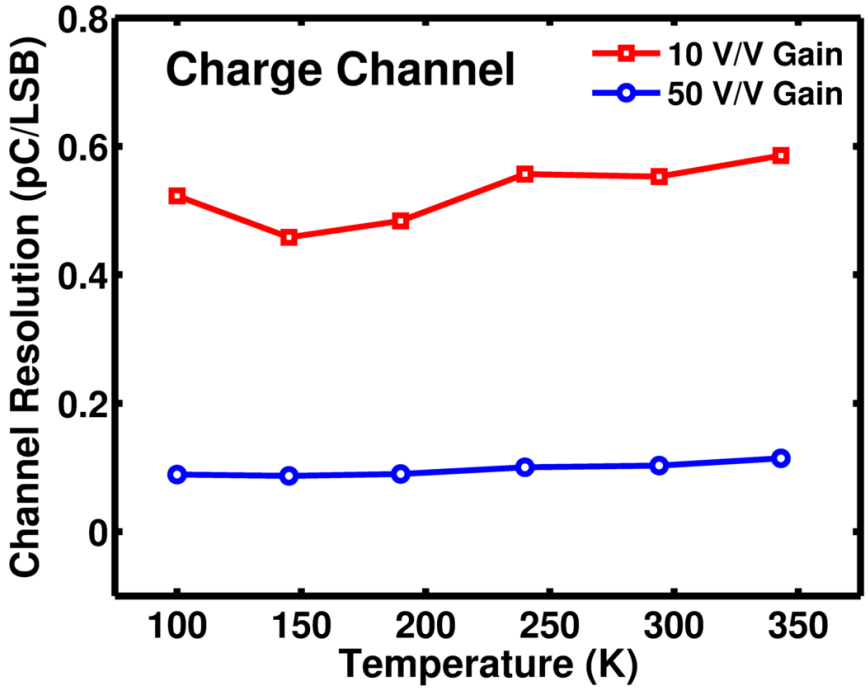

Figure 15. The charge channel resolution

Two major characteristics are evident. The gain is remarkably flat, showing little dependence on temperature over an almost 250°C temperature spread. In addition, the resolution is very tight. In the case of the universal and high-speed channels in the highest gain states, an LSB represents less than 10 mΩ. Even in the lowest gain, an LSB is less than 60 mΩ. For the charge channel in the high gain state, the resolution is approximately 0.1 pC per LSB, and it stays below 0.6 pC per LSB in the low gain state.

Along with resolution, channel noise was measured over the same temperature range. The noise data and the resulting sensitivity can be seen in Figures 16–18.

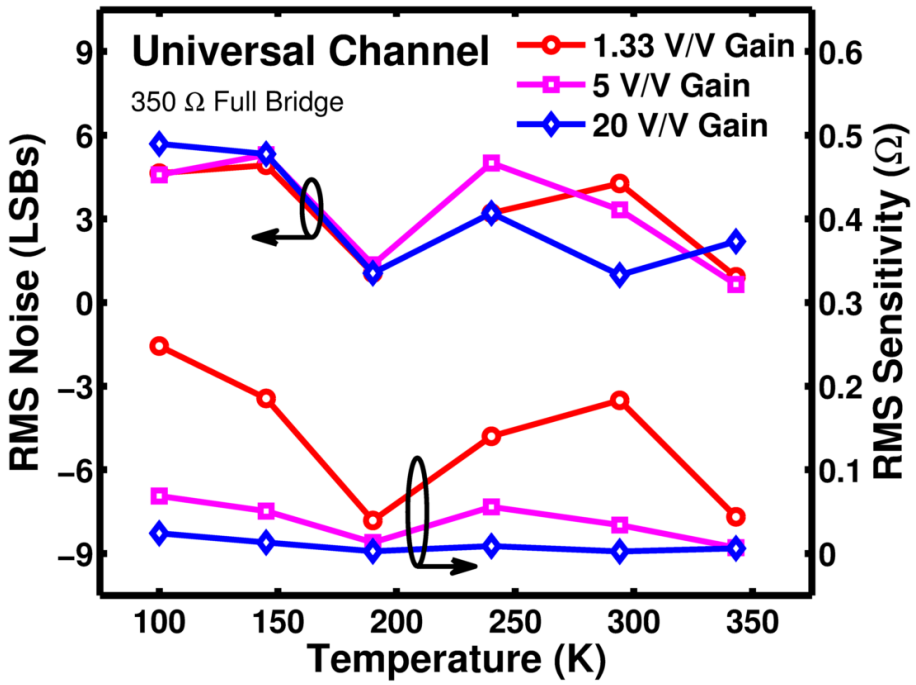

Figure 16. Universal channel noise and sensitivity

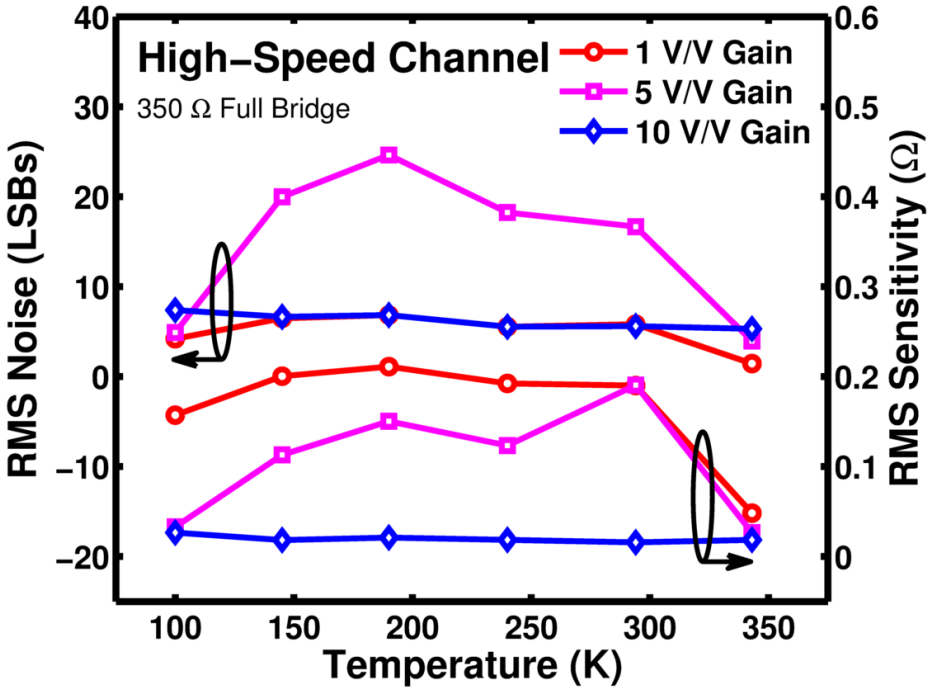

Figure 17. High-speed channel noise and sensitivity

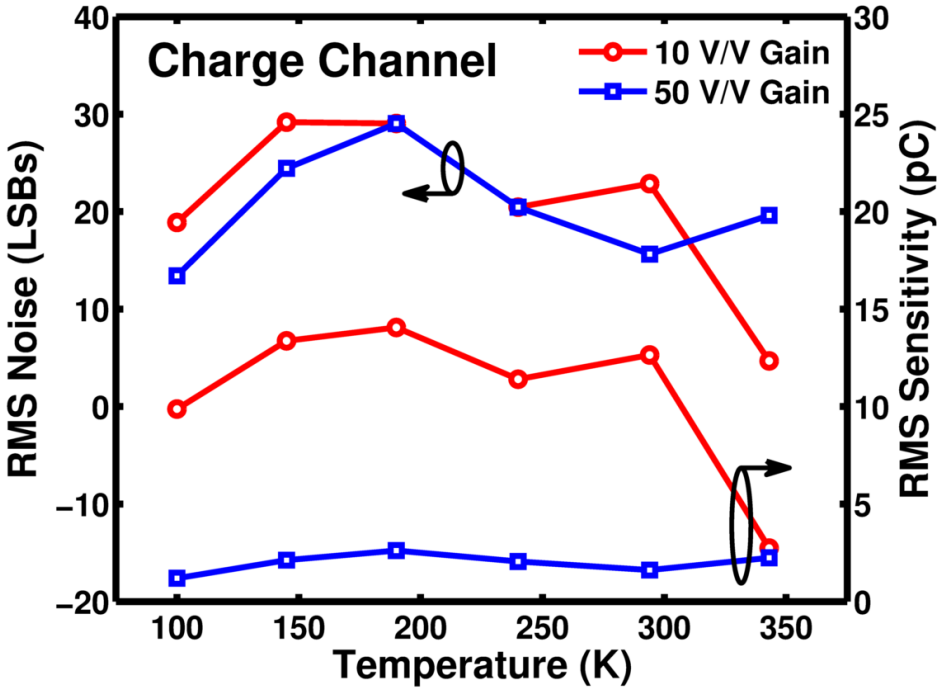

Figure 18. Charge channel noise and sensitivity

Except for occasionally falling off at the top and bottom ends of the temperature range, the noise levels stay fairly uniform for each gain state and falls far below the full scale range of 4096 LSBs. The universal channel had the best noise performance, staying below 6 LSBs over the entire temperature range. The high-speed and charge channels were consistently below 30 LSBs. A 6 and 30 LSB noise floor would result in a single, full-scale tone signal to noise ratio (SNR) of 47 and 33 dB, respectively.

Sensitivity was calculated from the product of the noise and resolution. It represents the input-referred noise source and can be interpreted as the measurement noise floor of the channel. Even in the lowest gain states, it stays below 0.25 Ω across the 243 K temperature range. In the higher gain states, it improves to below 50 mΩ, meaning that this REU implementation can reliably detect any change above 50 mΩ in resistance at any temperature between 100 and 343 K. For the charge channel, sensitivity stays better than 15 pC and 5 pC in the low and high gain states, respectively.

CHAPTER 7

REMOTE SENSOR INTERFACE IN RADIATION ENVIRONMENT

The RSI was subjected to TID exposure at Vanderbilt University and SEE testing over temperature at the Cyclotron Institute at Texas A&M University. A TID exposure of 100 krad revealed no observable degradation in the RSI operation. Noise values and supply currents were not noticeably altered between pre- and post-exposure.

Over-temperature SET Analog Noise Quantization

To quantify the effects of single event transients (SETs) on the RSI, the same noise measurements from the original over-temperature characterization were performed while the RSI was being subjected to broad beam irradiation using a variety of heavy ions and exposure temperatures. The test setup utilized the radiation dewar described in the previous section. The RSI was exposed from 85 K to 293 K. The heavy ions used were ^{20}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe. After factoring in the energy losses in air and through the Aramica windows using TRIM [22], the resulting surface linear energy transfer (LET) values were 2.5, 8.3, 29, and 57 MeV-cm2/mg, respectively. We observed an overall trend of higher noise level with increasing LET. The effect was observable at lower LETs, but became more significant with LETs above 20 MeV-cm2/mg, as shown in Figure 19.

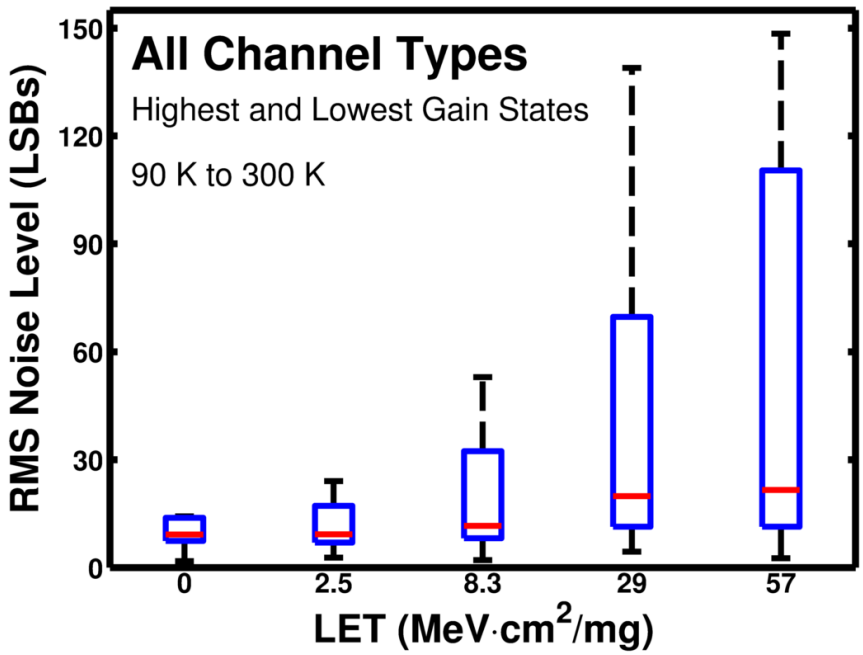

Figure 19. A box and whisker plot showing noise levels across all temperatures and channel types for the higest and lowest gain states

High Temperature SEL Experiment

The worst-case single event latchup (SEL) conditions for the RSI were a non-zero angle of ion incidence at high temperature under the highest LET ion possible. The RSI was exposed at 125°C to a fluence of 1.0 x 107 ions/cm2 of 129Xe ions at three different angles of incidence: 0°, 30° and 45° (LET = 47.3 MeV-cm2/mg at 0°). Currents were monitored in real-time with an Agilent® 6624A four-channel power supply set to detect any rise above critical limits. Throughout the test, no latchup was observed; supply currents stayed within safe tolerance, and throughout all radiation experiments (TID, SET Noise, and SEL) no catastrophic failures ever occurred, indicating that the RSI is SEL immune, as intended.

CHAPTER 8

REU MULTI-CHIP MODULE PACKAGING

A multi-chip module (MCM) packaging approach was selected for the final SiGe REU dual-ASIC implementation. The MCM methodology eliminates the need for PCB interconnects between the individual die (an interface failure opportunity) and also reduces the size and weight of the system implementation.

With an approximately 300°C operating temperature range for lunar applications, the packaging design philosophy was to match the coefficient of thermal expansion (CTE) of the packaging materials wherever possible. The stress on an interface is directly proportional to the difference in CTE between the materials and the change in temperature during thermal excursions.

The team considered multiple package material options: Si_3N_4, metal (Kovar®) and ceramic (AlN and Al_2O_3). Si_3N_4 had a matched CTE with Si, but it had a low technology readiness level (TRL) and was costly for our low volume work. Metal packages were commercially available but had an unacceptably mismatched CTE with Si. AlN would have provided a desirable CTE, but custom AlN packages were unavailable. In the end, a ceramic, Al_2O_3 package was selected as a median trade-off between cost, CTE, and availability.

The interconnect substrate technology was multilayer thin film copper and polyimide deposited and patterned on a base substrate [23] (see drawing in Figure 20).

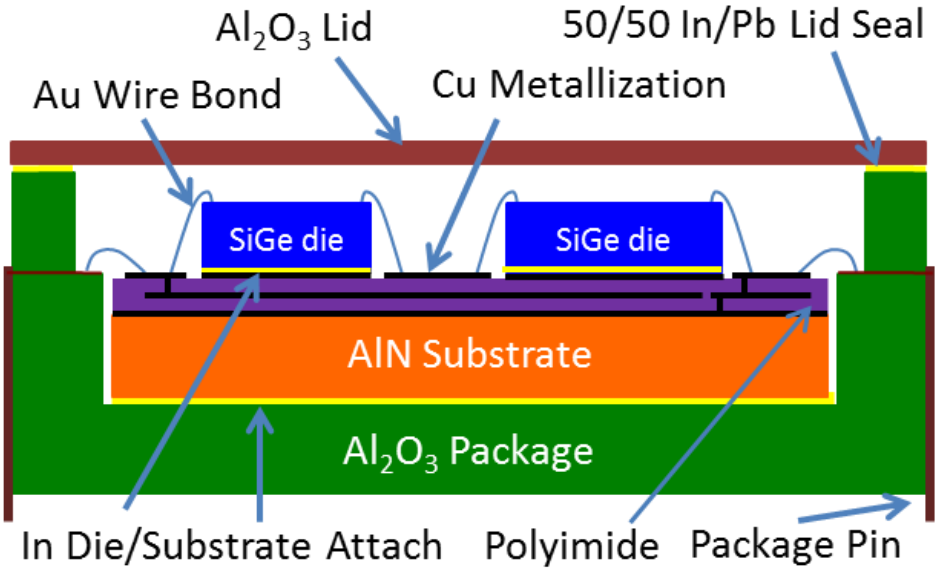

Figure 20. Drawing of the objects and materials used in the MCM

The polyimide was HD Microsystems PI-2611. Electroplated Cu was selected for its electrical conductivity and elongation. The AlN substrate provided an intermediate CTE between the Si die and the Al_2O_3 package (see Table 2).

Table 2. Comparison of CTE for selected packaging materials

	Si (SiGe Die)	*AlN*	*Al_2O_3*
CTE	2.8 ppm/ °C	4.5 ppm/ °C	6.7 ppm/ °C

A novel indium-based metallurgy was used as both the die and substrate attachment material. Indium remains malleable to cryogenic temperatures and helped relieve the strain between the substrate and package. Thermosonic Au wire bonding was used for die to substrate and substrate to package electrical interconnection because it has better fatigue resistance than Al wire. A metallized Al_2O_3 lid was solder sealed with 50/50 In/Pb solder to provide a hermetic package.

REU MCM Substrate Layout

The MCM net list was determined by the connections required between the analog and digital chips, the required package I/O, connections to the passive components, and power nets. In addition to the die, the package included passive components and a quartz oscillator for in-package clock generation. The substrate dimensions were determined by the cavity size of the Al2O3 quad flat package and were 36.58 mm x 36.58 mm, which gave a clearance of 0.5 mm to the inside edge of the package cavity.

After reviewing the net and component lists, the team decided that only a single signal layer was required and that two split planes would be included to provide low impedance power distribution. The power and ground planes were split to provide the different voltages (and return paths) required by the two SiGe die and came with the advantage of adding decoupling capacitance where they overlapped.

The top (signal) layer is shown in Figure 21.

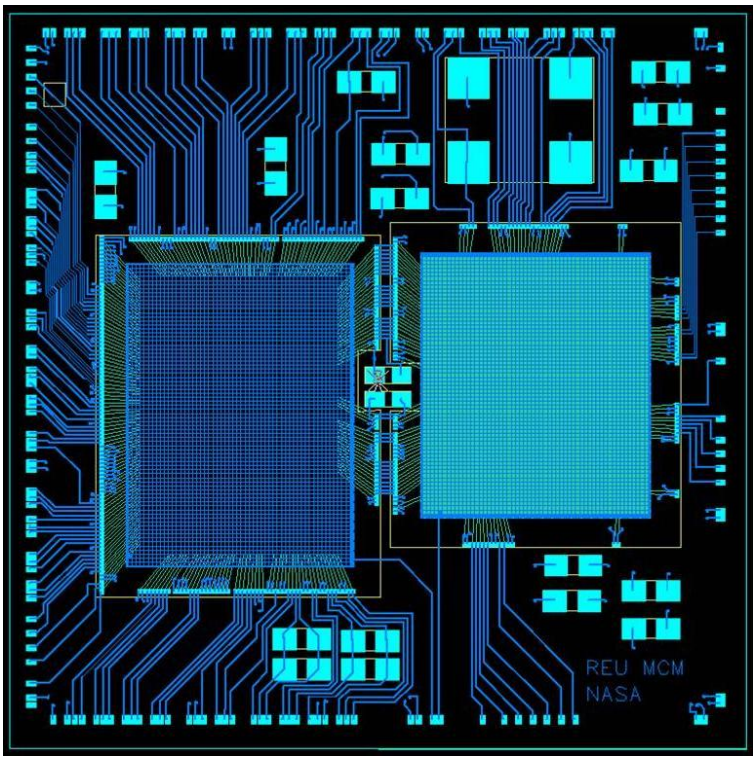

Figure 21. Layout capture of the top (signal) layer of the MCM substrate

The signals routed easily without crossovers or an extra metal layer due to the careful design of the two ASICs such that all chip interconnects could be directly connected, all package level I/Os could be routed straight to the outside, and all rail signals could be directly attached to the power and ground planes. Careful attention was also given to those planes, insuring that they could be generated as a solid blocks without any extensions or extra routing.

Each of the layers was separated by a 6.5 µm thick, low stress polyimide with etched vias for interconnection. The final populated and board-attached package is shown in Figure 22.

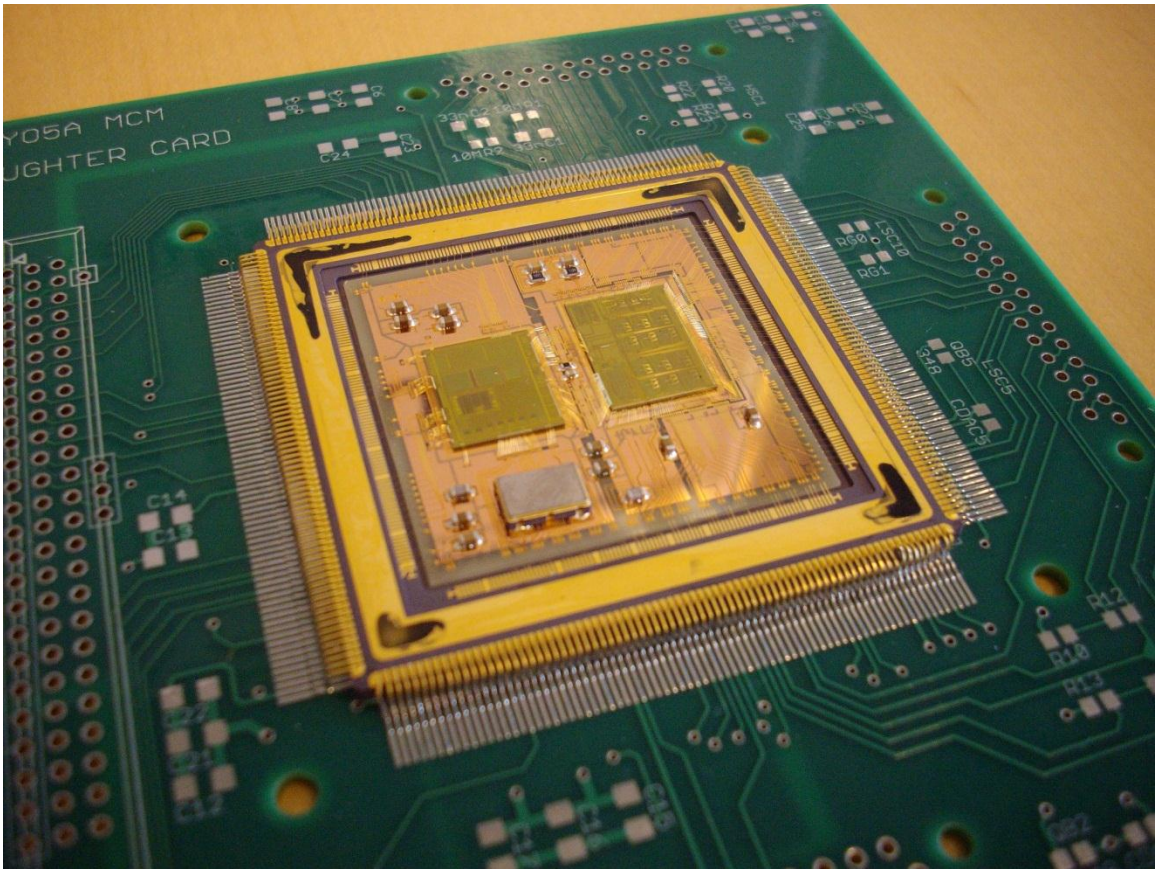

Figure 22. A photograph of an assembled MCM REU attached to a PCB with the lid removed

CHAPTER 9

INSERTION OPPORTUNITIES

The REU and underlying SiGe extreme temperature circuit library and technology developed during this work have numerous opportunities for insertion into spaceflight missions. While the ability of the SiGe REU to address specific mission requirements will be based on individual needs, the desire for small size, weight and power (SWaP) is almost universal, particularly in the area of spacecraft health monitoring functions. In addition, the ability to support operation outside of a controlled environment makes placement of the REUs on spacecraft far more flexible than existing solutions.

The SiGe REU will be at home in planetary operations, such as in the series of robotic rovers currently used to explore the Martian landscape. Again, in this case the combination of small size, low weight, and low power dissipation is highly desirable, and the additional gain in efficiency achieved by eliminating the need for the "warm box" will allow for additional allocation to scientific equipment. As a result, the next generation of Mars rovers would be an obvious insertion opportunity for SiGe extreme environment technology. This technology can be used not only for the REU, but also for other functions, such as communications, with additions to the existing circuit library.

SiGe technology will be equally at home on deep space exploration missions, such as the proposed flagship mission to Europa where support for cryogenic temperatures and radiation tolerance will be of critical importance. The Keck study commissioned during 2010 explored the requirements of the Titan mission including the applicability and value of SiGe technology to this program [24].

Some of the near-term opportunities for infusion of SiGe technology include

- Lunar Geophysical Network (several small landers throughout the lunar surface)

- Lunar South Pole-Aitken Basin Sample Return (lander to explore surface floor of dark polar craters for ice)
- Mars Sample Return mission
- Jupiter Europa Orbiter
- Trojan Tour and Rendezvous

CHAPTER 10

CONCLUSION

This thesis has presented the architecture, simulation, packaging, and over-temperature and radiation testing of a complex, 16-channel, extreme environment capable, SiGe Remote Electronics Unit containing the Remote Sensor Interface ASIC that can serve a wide variety of space-relevant needs as designed. These include future missions to the Moon and Mars, with the additional potential to operate in other hostile environments, including lunar craters and around the Jovian moon, Europa. It has shown the validity of the chip design and performance over an almost 250 K temperature range, down to 100 K, under 100 krad TID radiation exposure, with SEL immunity and operability in a high-flux SET environment.

The novelty of this work is the comprehensive, ground-up generation of new extreme environment design methodologies, culminating in the creation of a new state-of-the-art system-in-package that, for the first time, enables decentralized electronics throughout space-based vehicles without temperature control or shielding. The implication is that the elimination of restrictive, wasteful wiring and protection schemes will enable lighter and more capable space-based systems.

CHAPTER 11

FUTURE WORK

Outside of the current insertion opportunities presented in a previous chapter, this work has some obvious extensions. First, additional testing methods could provide results for resolution, noise, and sensitivity over the full temperature range. This could be accomplished by replacing the last copper ribbon cable with a cryogenic cable. The resistive loses of the cryogenic wire could be mitigated by adjusting the feedback scheme for the voltage regulators. Second, when the RDC ASIC come back out of fabrication, the testing could be repeated with a dual-ASIC implementation of the REU. Testing methods would be similar to those presented in this thesis. Lastly, the REU itself could move from a wired bus to a wireless network. For a minimal increase in Si real-estate, the current wire-line transceiver could be replaced with a wireless transceiver, thereby eliminating further wiring requirements in the space-based system as a whole.

REFERENCES

[1] NASA/JPL-Caltech/LMSS, "Setting up Juno's Radiation Vault," ed, 2010.

[2] A. S. Keys, J. H. Adams, M. C. Patrick, M. A. Johnson, and J. D. Cressler, "A review of NASA's Radiation-Hardened Electronics for Space Environments Project," in *2008 Space Conf.*, San Diego, CA, United States, 2008.

[3] R. M. Diestelhorst, S. Finn, L. Najafizadeh, M. Desheng, X. Pengfei, C. Ulaganathan, J. D. Cressler, B. Blalock, F. Dai, A. Mantooth, L. Del Castillo, M. Mojarradi, and R. Berger, "A monolithic, wide-temperature, charge amplification channel for extreme environments," in *IEEE Aerospace Conf.*, 2010, pp. 1-10.

[4] C. Ulaganathan, N. Nambiar, B. Prothro, R. Greenwell, S. Chen, B. J. Blalock, C. L. Britton, M. N. Ericson, H. Hoang, R. Broughton, K. Cornett, G. Fu, H. A. Mantooth, J. D. Cressler, and R. W. Berger, "A SiGe BiCMOS instrumentation channel for extreme environment applications," in *Midwest Symp. on Circuits and Systems*, 2008, pp. 217-220.

[5] J. D. Cressler, "Silicon-Germanium as an Enabling Technology for Extreme Environment Electronics," *IEEE Trans. on Device and Materials Reliability*, vol. 10, pp. 437-448, 2010.

[6] J. D. Cressler, J. H. Comfort, E. F. Crabbe, G. L. Patton, J. M. C. Stork, J. Y. C. Sun, and B. S. Meyerson, "On the Profile Design and Optimization of Epitaxial Si- and SiGe-Base Bipolar Technology for 77 K Applications. I. Transistor DC Design Considerations," *IEEE Trans. on Electron Devices*, vol. 40, pp. 525-541, 1993.

[7] J. D. Cressler, E. F. Crabbe, J. H. Comfort, J. M. C. Stork, and J. Y. C. Sun, "On the Profile Design and Optimization of Epitaxial Si- and SiGe-Base Bipolar Technology for 77 K Applications. II. Circuit performance issues," *IEEE Trans. on Electron Devices*, vol. 40, pp. 542-556, 1993.

[8] A. J. Joseph, J. D. Cressler, and D. M. Richey, "Operation of SiGe Heterojunction Bipolar Transistors in the Liquid-Helium Temperature Regime," *IEEE Electron Device Letters*, vol. 16, pp. 268-270, 1995.

[9] L. Najafizadeh, J. S. Adams, S. D. Phillips, K. A. Moen, J. D. Cressler, S. Aslam, T. R. Stevenson, and R. M. Meloy, "Sub-1-K Operation of SiGe Transistors and Circuits," *IEEE Electron Device Letters*, vol. 30, pp. 508-510, 2009.

[10] D. B. Thomas, L. Najafizadeh, J. D. Cressler, K. A. Moen, and N. Lourenco, "Optimization of SiGe bandgap-based circuits for up to 300 °C operation," *Solid-State Electronics*, vol. 56, p. 9, 2010.

[11] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Boston, MA: Artech House, 2003.

[12] A. P. G. Prakash, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. Andrews, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "The Effects of Irradiation Temperature on the Proton Response of SiGe HBTs," *IEEE Trans. on Nuclear Science*, vol. 53, pp. 3175-3181, 2006.

[13] R. Garbos and W. Mouyos, "X-33/RLV System Health Management/Vehicle Health Management," in *Proc. of the 1998 39th AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics, and Materials Conf.and Exhibit and*

AIAA/ASME/AHS Adaptive Structures Forum, Long Beach, CA, USA, 1998, pp. 1857-1864.

[14] R. Garbos-Sanders, L. Melvin, B. Childers, and B. Jambor, "System health management/vehicle health management for future manned space systems," in *AIAA/IEEE Digital Avionics Systems Conf.*, 1997, pp. 8.5-8-8.5-17.

[15] R. Berger, R. Garbos, J. Cressler, M. Mojarradi, L. Peltz, B. Blalock, W. Johnson, N. Guofu, F. Dai, A. Mantooth, J. Holmes, M. Alles, and P. McClusky, "Miniaturized Data Acquisition System for Extreme Temperature Environments," in *IEEE Aerospace Conf.*, 2008, pp. 1-12.

[16] "CAN Specification 2.0," ed. Stuttgart: Robert Bosch GmbH, 1991, p. 70.

[17] K. Meekins, D. Ferguson, and M. Basta, "Delay insensitive NCL reconfigurable logic," in *IEEE Aerospace Conf.*, 2002, pp. 4-1961-4-1966 vol.4.

[18] B. Hollosi, M. Barlow, F. Guoyuan, C. Lee, D. Jia, S. C. Smith, H. A. Mantooth, and M. Schupbach, "Delay-insensitive asynchronous ALU for cryogenic temperature environments," in *Midwest Symp. on Circuits and Systems*, 2008, pp. 322-325.

[19] C. Webber, J. Holmes, M. Francis, R. Berger, A. Mantooth, A. Arthurs, K. Cornett, and J. D. Cressler, "Event driven mixed signal modeling techniques for System-in-Package functional verification," in *IEEE Aerospace Conf.*, 2010, pp. 1-16.

[20] R. E. Harr and A. G. Stanculescu, *Applications of VHDL to circuit design*. Boston: Kluwer Academic, 1991.

[21] V. Ramachandran, M. J. Gadlage, J. R. Ahlbin, M. L. Alles, R. A. Reed, B. L. Bhuva, L. W. Massengill, J. D. Black, and C. N. Foster, "Application of a novel test system to characterize single-event transients at cryogenic temperatures," in *Int. Semiconductor Device Research Symp.*, 2009, pp. 1-2.

[22] J. F. Ziegler and J. P. Biersack, *Srim - the Stopping and Range of Ions in Matter*: Ziegler Scientific Company, 2008.

[23] S. Sivaswamy, W. Rui, C. Ellis, M. Palmer, R. W. Johnson, P. McCluskey, and K. Petrarca, "System-in-package for extreme environments," in *Electronic Components and Technology Conf.*, 2008, pp. 2044-2050.

[24] J. R. Greer, J. M. Jackson, J. I. Lunine, and M. M. Mojarradi. (2011, Future Missions to Titan: Scientific and Engineering Challenges.